1 / 3

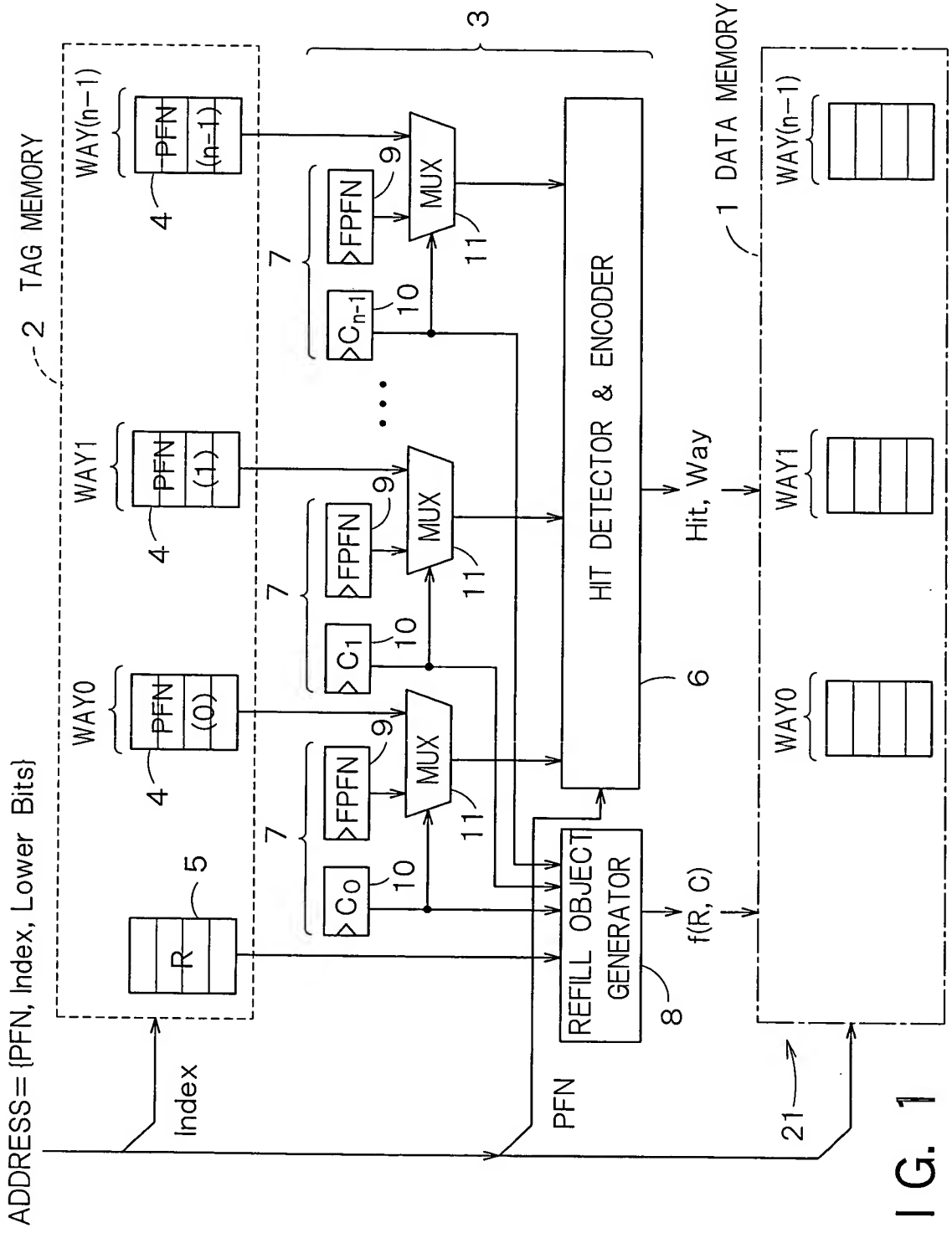
ADDRESS= {PFN, Index, Lower Bits}
Index
2 TAG MEMORY
WAY(n-1)
WAY1
WAY0
PFN (n-1)
PFN (1)
PFN (0)
4
5
R
7
FPFN
9
10
C_{n-1}
C_1
C_0
MUX
11
3
HIT DETECTOR & ENCODER
6
Hit, Way
REFILL OBJECT GENERATOR
8
f(R, C)
PFN
21
1 DATA MEMORY
WAY(n-1)
WAY1
WAY0

FIG. 1

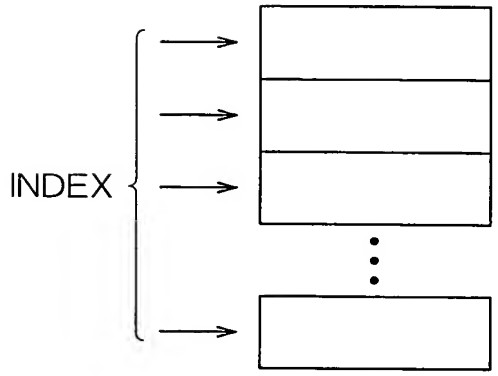

FIG. 2

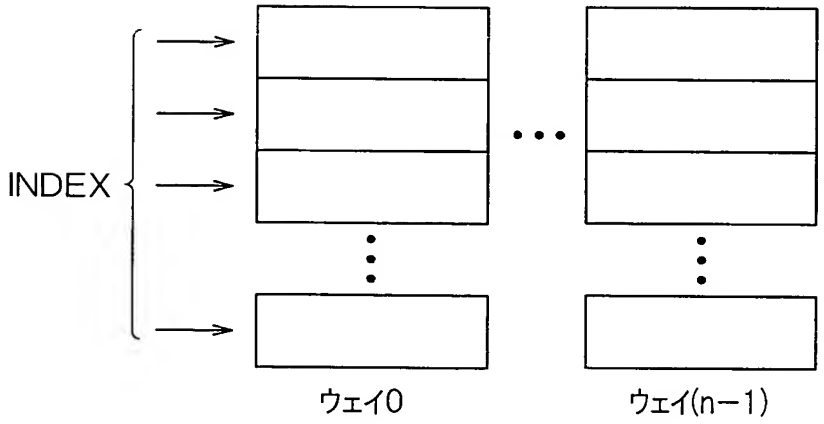

FIG. 3

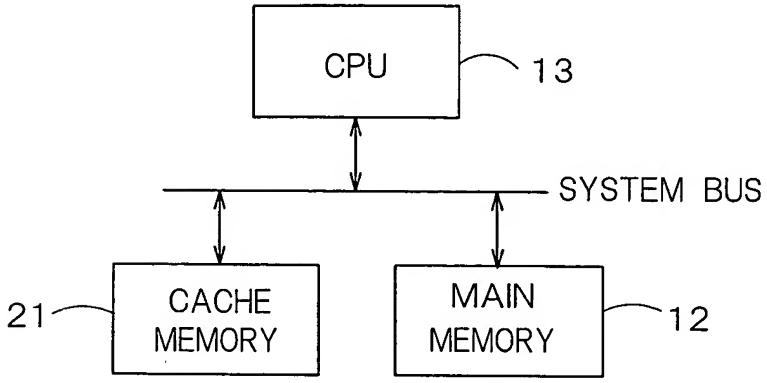

FIG. 4

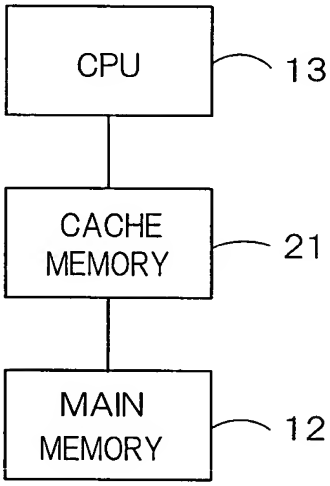

FIG. 5

```
S1;          la   rA,  0×60000001
S2;          sw   rA,  R0
S3;          la   rA,  0×60000000
S4;   Loop : sw   r0,  rA
S5;          addi rA,  rA,  4
S6;          addi Rc,  Rc,  -1
S7;          bne  Rc,  $0,  Loop
```

FIG. 6